FPGA-BASED DIGITAL PROCESSING UNIT FOR SPICA SAFARI

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Abstract

This paper describes a prototype board developed at IFSI in the framework of the SAFARI DPU feasibility study. The breadboard is based on an FPGA where the main DPU processor — a Leon System on Chip — can be implemented. The breadboard provides the memory, connectivity and expandability resources that make it a suitable platform for exploring and evaluating a wide range of HW/SW configurations, as required during the early design phases of the Safari Instrument Control Unit. The main characteristics of the proposed processor and the tests performed are described as well.

Key words: DPU, FPGA, SpaceWire, Processor, Leon

1. Introduction

The SAFARI Warm Electronics is located in the SPICA Service Module and includes:

− DCU = Detectors Control Unit
− MCU = Mechanism Control Unit
− CCU = Cooler Control Unit
− DPU = Digital Processing Unit

This paper focuses on the DPU, which is in charge of the overall instrument control, and has data interfaces with all the three other units of the Warm Electronics (DCU, MCU, CCU) and with the SpaceCraft (S/C). The DPU is responsible for the following activities:

− Telemetry and Telecommand exchange with the S/C
− Instrument Commanding, based on the received and interpreted Telecommands
− Instrument monitoring and control, based on the Housekeeping data acquired from the instrument units
− Detectors readout data acquisition, preprocessing and formatting according to the Telemetry protocol
− Synchronization of all the instrument activities

These activities will be carried out by the DPU On Board Software, which will be implemented as a real time multitask application running on a microprocessor. To meet the mass and size budgets, a compact HW architecture based on the use of an FPGA has been studied.

In the following, Section 2 discusses the proposed processor for the SAFARI DPU and reports considerations on the usage of FPGAs for its implementation; Section 3 introduces the SpaceWire standard and its use for on board communications; Section 4 describes the breadboard that has been developed, and the tests performed with it are discussed in Section 5.

2. Leon SoC and FPGA implementation

The DPU processor must be a high performance, reliable, radiation hardened microprocessor. These requirements are met by the Leon2-FT processor, which is the result of ESA's efforts in the development of processors for space applications. Leon is a 32-bit processor compliant with the SPARC V8 architecture. It is based on the AMBA AHB and APB buses and is particularly suitable for system-on-a-chip (SOC) designs.

The Leon2-FT (Fault Tolerant) SoC is available both as VHDL soft cores for implementation on radiation tolerant FPGAs and as a rad-hard ASIC from Atmel (AT697 component). For implementation on an FPGA, the Leon2-FT SoC can be obtained from ESA (in the frame of ESA-funded activities) as a library of VHDL IP cores, comprising not only the CPU core but also many other modules and peripherals required to build up a complete SoC like the one shown in the block diagram of Figure 1. The Leon SoC VHDL model is fully synthesizable and technology independent, i.e. it supports implementation on FPGAs from different vendors.
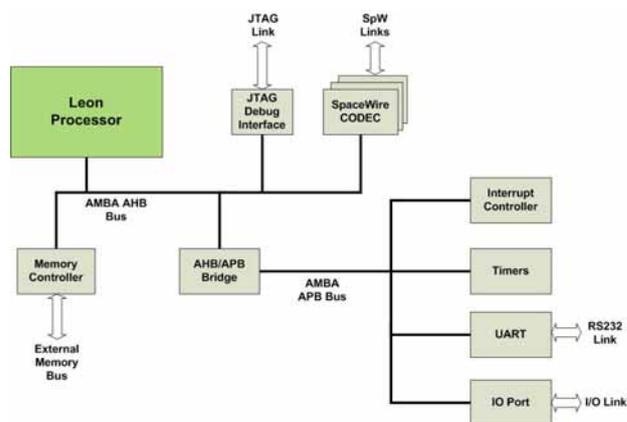

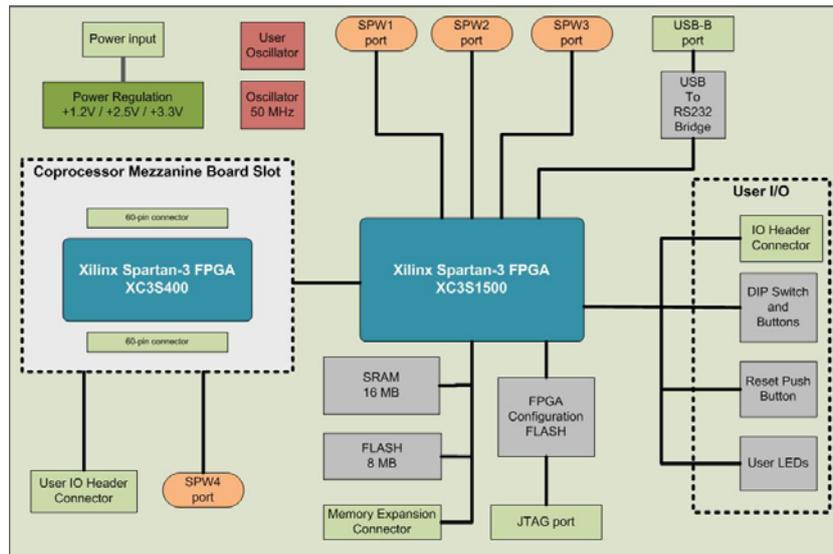Figure 1: Example SoC based on the Leon processor.

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Figure 2: BreadBoard Block Diagram.

The FPGA approach maximizes the designer's freedom to customize the SoC according to the specific application's needs. In fact the Leon processor and its peripherals are highly configurable through VHDL generics, and peripherals can be added/removed as required. For example, the exact required number of SpaceWire links can be included into the SoC design by instantiating a corresponding number of SpaceWire CODECs attached to the AHB system bus. Another advantage of the FPGA approach is that it enables easy hardware changes at any time during the development phase.

Leon2-FT features Fault Tolerance techniques provided at the design (VHDL) level, like TMR (Triple Modular Redundancy) protection on all flip-flops and EDAC protection for all memories. In addition, the adopted FPGA should be a radiation-tolerant FPGA, which are available from e.g. Actel and Xilinx. Such devices can be either reprogrammable or once-only-programmable.

Reprogrammable FPGAs (SRAM-based) allow in flight reconfiguration but cause the design to become more complex, because of the necessity to employ adequate mitigation techniques against SEUs in their on-chip configuration memory (Habinc et al., 2002; Fiethe et al., 2007). These mitigation techniques all have the side effect of requiring some amount of hardware overhead, and this should be taken into account when volume, mass and power budgets are critical.

Once-only-programmable FPGAs (based on anti-fuse technology), on the contrary, represent a well established solution for space applications. An example implementation on a one-time-programmable FPGA is the LEON3FT-RTAX, a product from Aeroflex-Gaisler, consisting in a Leon3-FT SoC implemented on a RTAX2000S, which is a radiation tolerant FPGA from Actel. This processor can be clocked at up to 24 MHz over the full military temperature range; this provides 20 DMIPS (Dhrystone MIPS) and the power consumption is typically 0.5W at full processor load. Radiation performance is the following: 300 Krad (functional) and 200 Krad (parametric) TID; SEL immune to a LET threshold of 117 MeVcm2/mg; SEU error rate better than 1E-10 errors per bit-day.

3. SpaceWire Interfaces

The data interfaces between the DPU and the DCU, MCU, CCU and the S/C are all expected to be implemented according to the SpaceWire standard (Parkes et al., 2003). This choice is driven by the need to facilitate the integration and testing of many units provided by different institutes/industries. Relying on a well known standard, for which extensive test and development equipment is available, goes in that direction.

The SpaceWire standard defines a data-handling network for use onboard spacecrafts, and it is being widely adopted on ESA, NASA and JAXA missions. SpaceWire provides serial, high-speed (2 Mbits/s to 200 Mbits/s), bidirectional, full-duplex, reliable data links. SpaceWire devices (CODECs and Routers) are available as both validated VHDL IP Cores and radiation tolerant ASICs.

Figure 3: Picture of the DPU BreadBoard developed at IFSI.
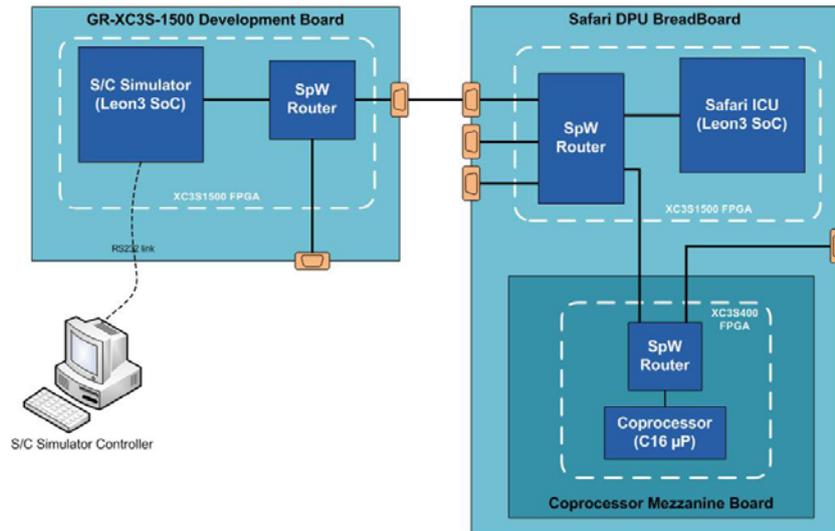
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Figure 4: A test set-up for the BreadBoard.

One of the key features of the SpaceWire protocol is its simplicity, which results in low gate-count CODEC (coder/decoder) implementations. This means that one or more SpaceWire interfaces can easily be included in an FPGA together with the microprocessor, i.e. as part of a SoC design. A SpaceWire CODEC can quite straightforwardly be included into a Leon SoC, by attaching it to the AMBA system bus. The ESA IP Cores library includes a VHDL core implementing the SpaceWire CODEC, with FIFOs and AMBA AHB master/slave interfaces, and with DMA capabilities to efficiently transfer packets between the SpW interface and the processor memory.

4. SAFARI DPU BreadBoard

The Safari DPU BreadBoard developed at IFSI is a versatile platform for the evaluation of systems based on the Leon processor. Figure 2 shows a block diagram of the board, while a picture of it is shown in Figure 3. A detailed list of the technical characteristics of the breadboard is given in Table 1.

The board includes a medium-size capacity FPGA from Xilinx (XC3S1500), which enables the implementation of complex designs, such as a Leon SoC plus a SpaceWire Router. The 4 SpaceWire ports available on the board provide connection capabilities to SpaceWire links, like those which will be used by the Safari DPU for communicating with the Spacecraft and the Subsystems. The amount of memory available on board (16 MB SRAM + 8 MB Flash) can be extended via a memory expansion connector. Furthermore, a mezzanine slot allows expansion to a coprocessor board, which can perform processing functions such as data compression algorithms, which might be required to reduce the size of science data, to cope with limited telemetry downlink capacity.

We note that for this breadboard we have chosen a non radiation tolerant Xilinx Spartan3 FPGA, since it is a low cost solution, and it is suitable for our architectural evaluation purposes. Moreover, Xilinx FPGA development is supported by a series of free software tools included in the Xilinx ISE WebPack[TM] Design Suite, which offers a complete design flow (synthesis, place&route, device programming, simulation).

5. Tests performed with the BreadBoard

In order to test the BreadBoard and familiarize with the Leon processor and the communication over SpaceWire, we have used the set-up shown in Figure 4, which involves the use of three electronics boards: the BreadBoard, a custom mezzanine board that has been plugged into the slot provided by the BreadBoard, and a GR-XC3S-1500 board (a development board produced by Gaisler Research and Pender Electronic Design).
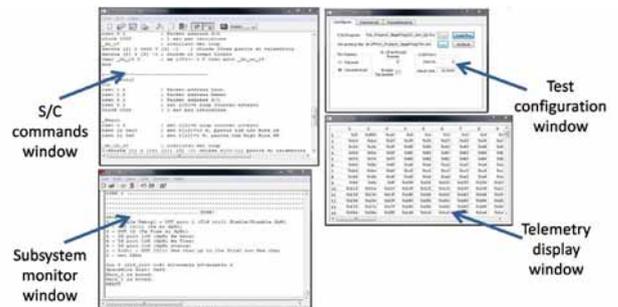

Figure 5: Graphical interface for test guidance from a host PC.

Each of the boards in the test set-up carries a processor and these processors have been connected to form a

Table 1: Technical details of the SAFARI DPU BreadBoard.

FPGA	- Xilinx Spartan-3 FPGA XC3S1500 (1.5 M gates) in a 456-pin BGA package
	- Xilinx Flash Proms for storage of FPGA configuration: XCF04S (4 Mbit) and XCF01S (1 Mbit)
Memory	- SRAM: 16 MB (4M x 32)
	- NOR Flash: 8 MB (configurable as 8M x 8 or 4M x 16)
	- Memory Expansion Connector (120 pin) (e.g. for addition of SDRAM modules)
Interfaces	- 3 SpaceWire Connectors for LVDS signals from the XC3S1500 FPGA
	- 1 SpaceWire Connector for LVDS signals from the Coprocessor Mezzanine Board
	- USB Connector to provide a RS232 link (through a USB-to-UART bridge controller)
	- JTAG connectors for both Parallel Cable III and Parallel Cable IV
Expandability	- Slot for the Coprocessor Mezzanine Board (two 20x3 pin female header connectors)
User IO	- Header connectors: 16 signals from XC3S1500 FPGA and 16 signals from Coprocessor Board
	- LEDs, DIP Switch and Push Buttons for user-definable functions
Power Regulators	- 3.3V (I/O), 2.5V (auxiliary), 1.2V (core) obtained from a single 5V power supply
Oscillators	- 50 MHz oscillator, plus an optional user-fitted oscillator
Board size	- 114 x 60 mm

SpaceWire network. This network is intended to mimic the connection between the SpaceCraft (S/C), the SAFARI DPU, and a DPU Coprocessor. A Leon3 SoC has been synthesized on the BreadBoard to play the role of the SAFARI DPU, and on the GR-XC3S-1500 board to play the role of the S/C. For the DPU coprocessor, a 16-bit microcontroller (C16, from www.opencores.org) has been implemented on the mezzanine board's FPGA. SpaceWire routers have been included into the various FPGA designs to provide the processors with multiple connection ports.

It should be noted that Leon3 is being used as the DPU processor in place of the Leon2-FT in this early stage evaluation. Leon3 is an IP SoC designed by Aeroflex Gaisler as an evolution of Leon2; it is freely downloadable in source code form from Aeroflex Gaisler's web pages under GNU GPL license. Software development for Leon3 is supported by a number of tools provided by the same company, such as cross-compilation tool chains, a target debugger, and simulators. Various RTOS (Real Time Operating Systems) are also available, among which the open source operating system RTEMS.

Application code has been written in C for the various processors in order to perform the tests; on Leon processors the multitasking environment has been provided by the Pthread library. A simple protocol has been devised on top of SpaceWire to enable the exchange of messages between the nodes of the network. Using this protocol, the S/C simulator node can send requests of data packets to the Safari DPU node or its coprocessor, which will reply accordingly.

The test execution can be driven and monitored from a host PC connected through a RS232 link to the S/C simulator node. In Figure 5 we show a snapshot of the graphical interface program running on the host PC. This program gives great flexibility in composing command packets and creating sequences of commands. Transmission of SpaceWire Time Codes from the S/C simulator to the rest of the network is also supported and has been tested.

REFERENCES

Parkes, S. M. et al., 2003, "ECSS-E-50-12A, SpaceWire Links, Nodes, Routers and Networks", European Cooperation for Space Data Standardization
Fiethe, B., Michalik, H., Dierker, C., Osterloh, B., Zhou, G. 2007, "Reconfigurable System-on-Chip Data Processing Units for Miniaturized Space Imaging Instruments", Proceedings of the Conference on Design, Automation and Test in Europe (DATE), ACM
Habinc, S., 2002, "Suitability of Reprogrammable FPGAs in Space Applications", Report ESA contract No. 15102/01/NL/FM(SC) CCN-3